CUSTOMER NO.
34456

IN THE SPECIFICATION

Please amend the specification at pages 4-5, paragraph 0015 as follows:

[0015] FIG. 1 illustrates in partial schematic and partial block diagram form a circuit 20 using a buffer 40 in accordance with the present invention. Circuit 20 includes generally a signal source 30, buffer 40, an interconnect line 50, and a load 60. Signal source 30 provides a time-varying (AC) signal to an output terminal thereof referenced to a ground terminal. Signal source 30 may be any number of circuits including a voltage controlled oscillator (VCO), an external clock or oscillator, an output of a radio frequency (RF) amplifier, a modulator, etc. Buffer 40 includes generally a capacitor 42, a P-channel metal-oxide-semiconductor (MOS) transistor 44, an N-channel MOS transistor 45, and a resistor 46. Capacitor 42 has a first terminal connected to the output terminal of signal source 30 at a node 41, and a second terminal connected to a ~~node 42~~ node 43. Transistor 44 has a source connected to a first power supply voltage terminal for receiving a first power supply voltage, a gate connected to the second terminal of capacitor 42 at node 43, and a drain connected to an output node 47. The first power supply voltage is a relatively low positive power supply voltage having a nominal value of about 1.2 volts. Transistor 45 has a drain connected to the drain of transistor 44 at node 47, a gate connected to the second terminal of capacitor 42 at node 43, and a source connected to a second power supply voltage terminal for receiving a second power supply voltage, designated ground, having a nominal voltage of about 0 volts. Resistor 46 has a first terminal connected to the second terminal of capacitor 42 at node 43, and a second terminal connected to the drains of transistors 44 and 45 at node 47. Interconnect line 50 has a first end connected to the drains of transistors 44 and 45 at node 47, and a second end. Load 60 is in the form of a capacitor having a first terminal connected to the second end of interconnect line 50, and a second terminal connected to ground.

Please amend the specification at page 5, paragraph 0016 as follows:

[0016] Buffer 40 translates an AC input signal having a relatively high peak-to-peak voltage swing on provided by signal source 30 to node 41 into a second signal having a smaller peak-to-peak voltage swing at node 47. In the illustrated embodiment the voltage swing on the signal at node 41 is about 3.5 volts, and the power supply voltage for buffer 40 is about 1.2 volts. Buffer 40 uses capacitive voltage division between the capacitance of capacitor 42 and the parasitic gate capacitances of transistors 44 and 45 to reduce this signal swing to about 1.2 volts (the first power supply voltage) or less. In one embodiment, transistors 44 and 45 have a gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process. Thus buffer 40 can use faster low-voltage transistors while reducing the loading seen by signal source 30 and hence power consumption.